Ordering number : EN4469A

Monolithic Linear IC



No. 4469A

LA4805V

3 V Stereo Headphone Power Amplifier

Overview

The LA4805V is a power IC developed for use in stereo headphones. It includes low frequency enhancement, beep function and output control circuits on-chip. Furthermore, the LA4805V realizes a high S/N ratio, a high ripple exclusion ratio, and low current drain.

Functions

- Stereo headphone power amplifier
- Low frequency enhancement (L.BOOST)
- Beep amplifier
- Output suppression circuit (PVSS)
- Power switch
- Muting switch

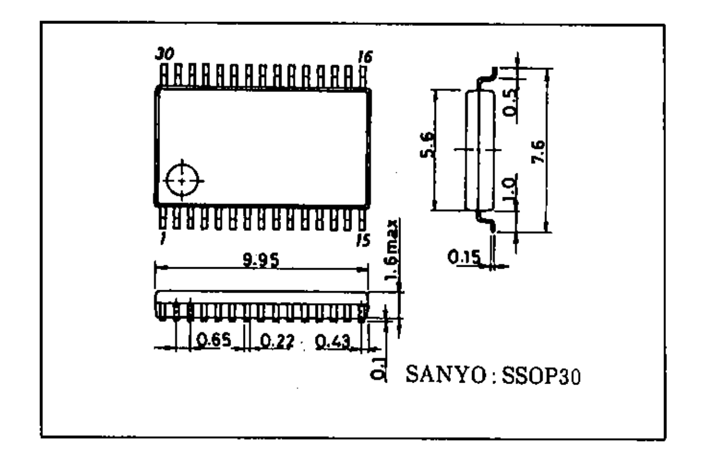
Features

- Low current drain (8.3 mA typical)
- High S/N ratio (90 dB typical, 13 µV)
- High ripple exclusion ratio (75 dB typical)
- No output electrolytic capacitors required
- Ultra-miniature package (SSOP-30)

Package Dimensions

unit: mm

3191-SSOP30



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{CC} max		4.5	V
Allowable power dissipation	Pd max		500	mW
Operating temperature	Topr		–15 to +50	°C
Storage temperature	Tstg		–40 to +150	°C

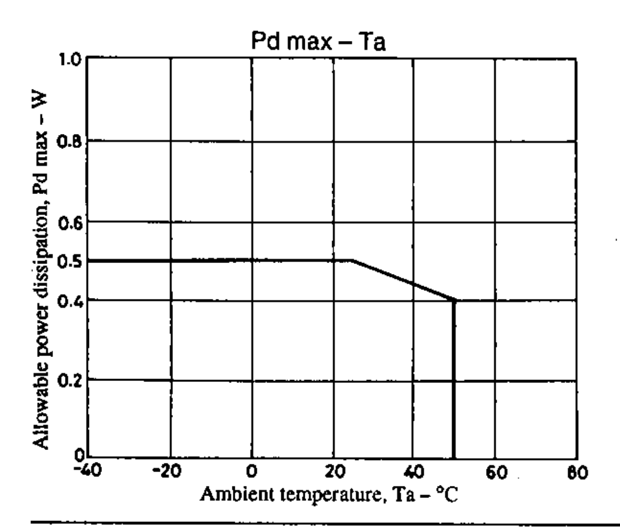
Operating Conditions at Ta = 25°C

Parameter	Symbol	Condition	Rating	Unit
Recommended supply voltage	V_{CC}		3.0	V
Recommended load resistance	R_L		16 to 32	Ω
Operating supply voltage range	V_{CC} op		1.8 to 3.6	V

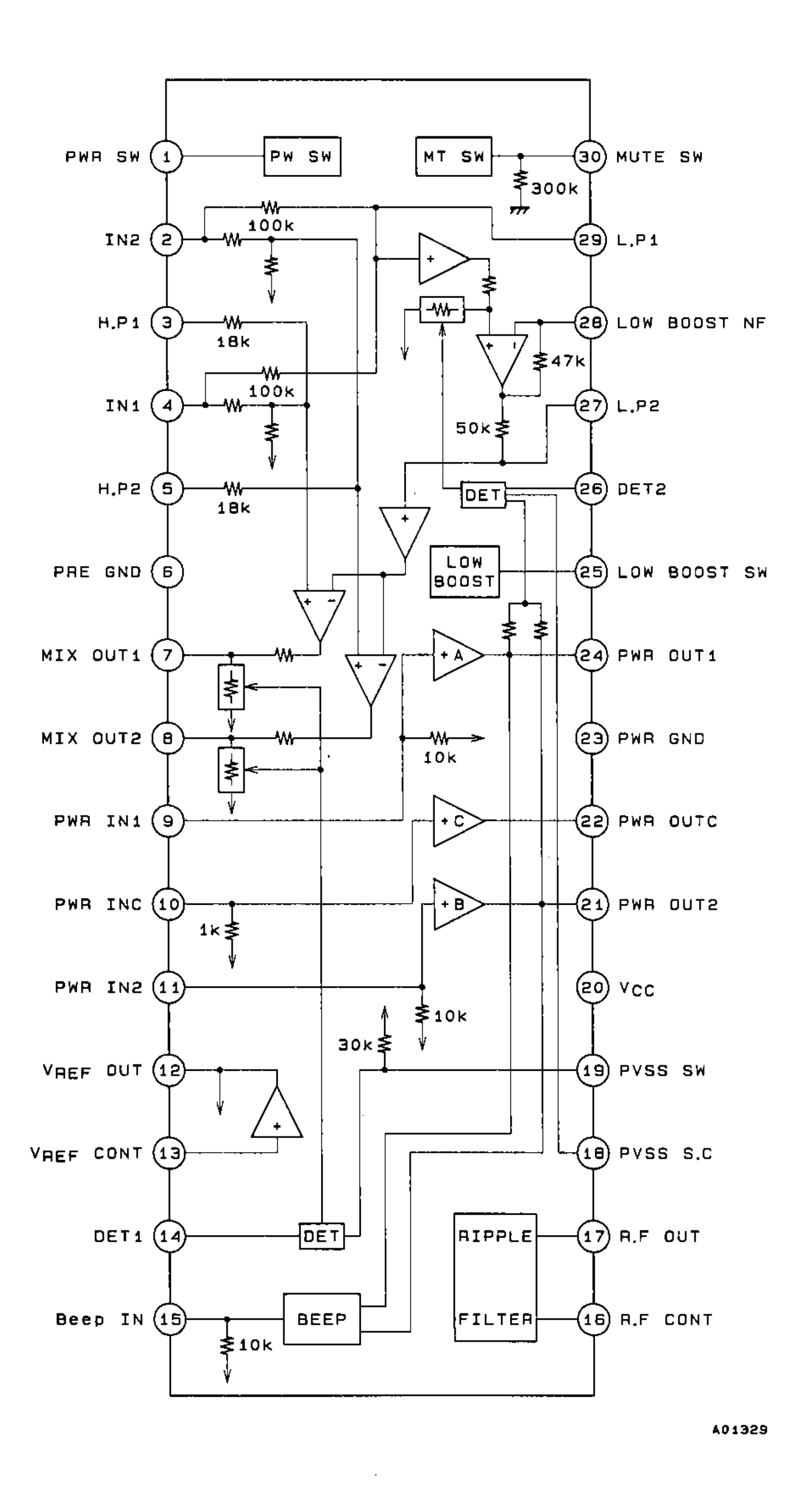
Operating Characteristics
at Ta = 25°C, V_{CC} = 3.0 V, f = 1 kHz, 0.775 V = 0 dBm, R_L = 10 kΩ (L.B), R_L = 16 Ω (PWR)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
[L.BOOST +PVSS + PWR]						
Quiescent current	$I_{CCO}1$	IC off		0.05	1.0	µA
	$I_{CCO}2$	Muting on	1.0	2.7	5.0	mA
	$I_{CCO}3$	Rg = 0, L.BST/PVSS off	4.0	8.3	12.0	mA
	$I_{CCO}4$	Rg = 0, L.BST/PVSS on	4.5	8.6	12.5	mA
[PWR AMP]						
Output power	P_O	THD = 10%	15	25		mW
Voltage gain	VG1	V_O = –10 dBm	15.7	17.7	19.7	dB
Channel balance	V_{BL}	V_O = –10 dBm	–1	0	1	dB
Total harmonic distortion	THD1	V_O = 0.35 V		0.1	0.3	%
Output noise voltage	$V_{NO}1$	Rg= 0, DIN AUDIO		13	25	µV
Crosstalk	CT1	V_O = –10 dBm, TUN = 1 kHz, Rg = 0	35	45		dB
Ripple exclusion ratio	SVRR1	V_{CC} = 1.8 V, f = 100 Hz, V_R = –20 dBm, TUN = 100 Hz	60	75		dB
Muting attenuation	ATT_M	THD = 1%, Rg = 0 kΩ	80	90		dB
Beep output	$V_{O\ BEEP}$	V_{IN} = –16 dBm (sine wave)	1.0	3.0		mV
Output current offset	$V_{DC\ OFF}$	V_{IN} = 0 V, Rg = 0	–20	0	20	mV
Input resistance	Ri		7	10	13	kΩ
[L.BOOST]						
Voltage gain	VG2	V_{IN} = –30 dBm, boost on/off	–3.2	–5.2	–7.2	dB
Boost*	L.BTS1	V_{IN} = –30 dBm, f = 100 Hz, boost on	13	15	17	dB
	L.BTS2	V_{IN} = –30 dBm, f = 10 kHz, boost on	3	5	7	dB
Maximum output voltage	V_O max	THD = 1%, boost on	0.2	0.4	0.6	V
Total harmonic distortion	THD2	V_O = 0.1 V, boost on		0.085	0.25	%
Crosstalk	CT2	V_O = –20 dBm, Rg = 0, boost on	25	30		dB
Output noise voltage	$V_{NO}2$	Rg = 0, boost off		3	10	µV
Ripple exclusion ratio	SVRR2	Rg = 0, f = 100 Hz, Vg = –20 dBm, boost on	50	60		dB
[L.BOOST + PWR]						
Voltage gain	VG3	V_{IN} = –30 dBm, f = 1 kHz, boost on/off	8	10	12	dB
Output voltage	V_O1	V_{IN} = –30 dBm, f = 100 Hz, boost on	0.13	0.23	0.33	V
Total harmonic distortion	THD3	V_{IN} = –30 dBm, f = 100 Hz, boost on		0.14	0.5	%
Crosstalk	CT3	V_O = –20 dBm, R_V = 0 Ω, boost on	25	32.5		dB
[L.BOOST + PVSS + PWR]: When V_O1 is maximum						
PVSS voltage	$V_{O\ PVSS}2$	V_{IN} = –30 dBm, PVSS2	–32.5	–37.5	–42.5	dBm
PVSS width	$V_{O\ PVSS}\ W$	The input amplitude when the output is +3 dB over the starting point	25	30	35	dB
PVSS distortion	THD_{PVSS}	V_{IN} = –40 dBm, PVSS2		0.55	2.0	%
PVSS starting input	$V_{IN\ PVSS}$	PVSS2	–41	–46	–51	dBm


Note: • Boost levels relative to 1 kHz

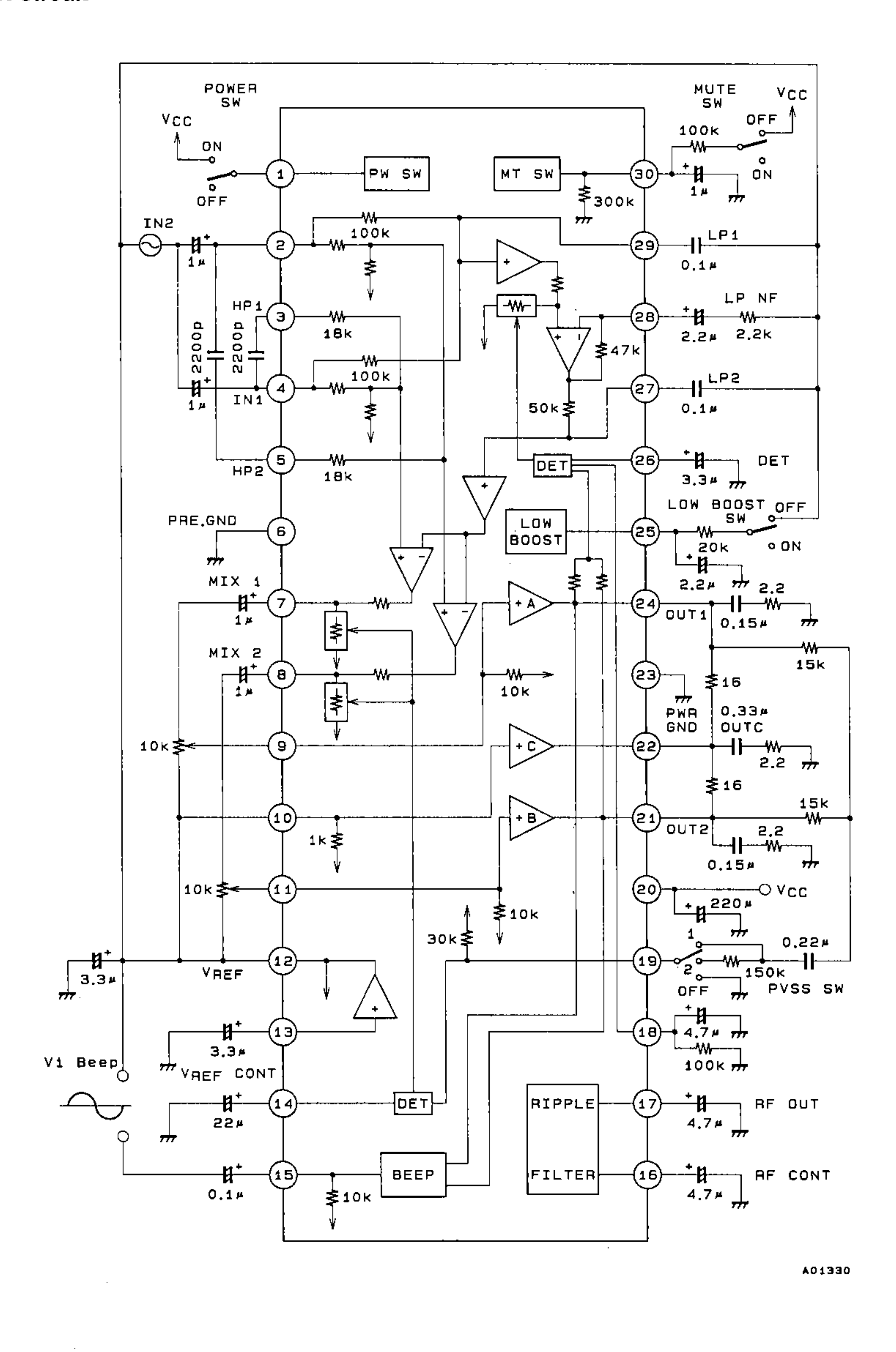


Pin Assignment and Block Diagram



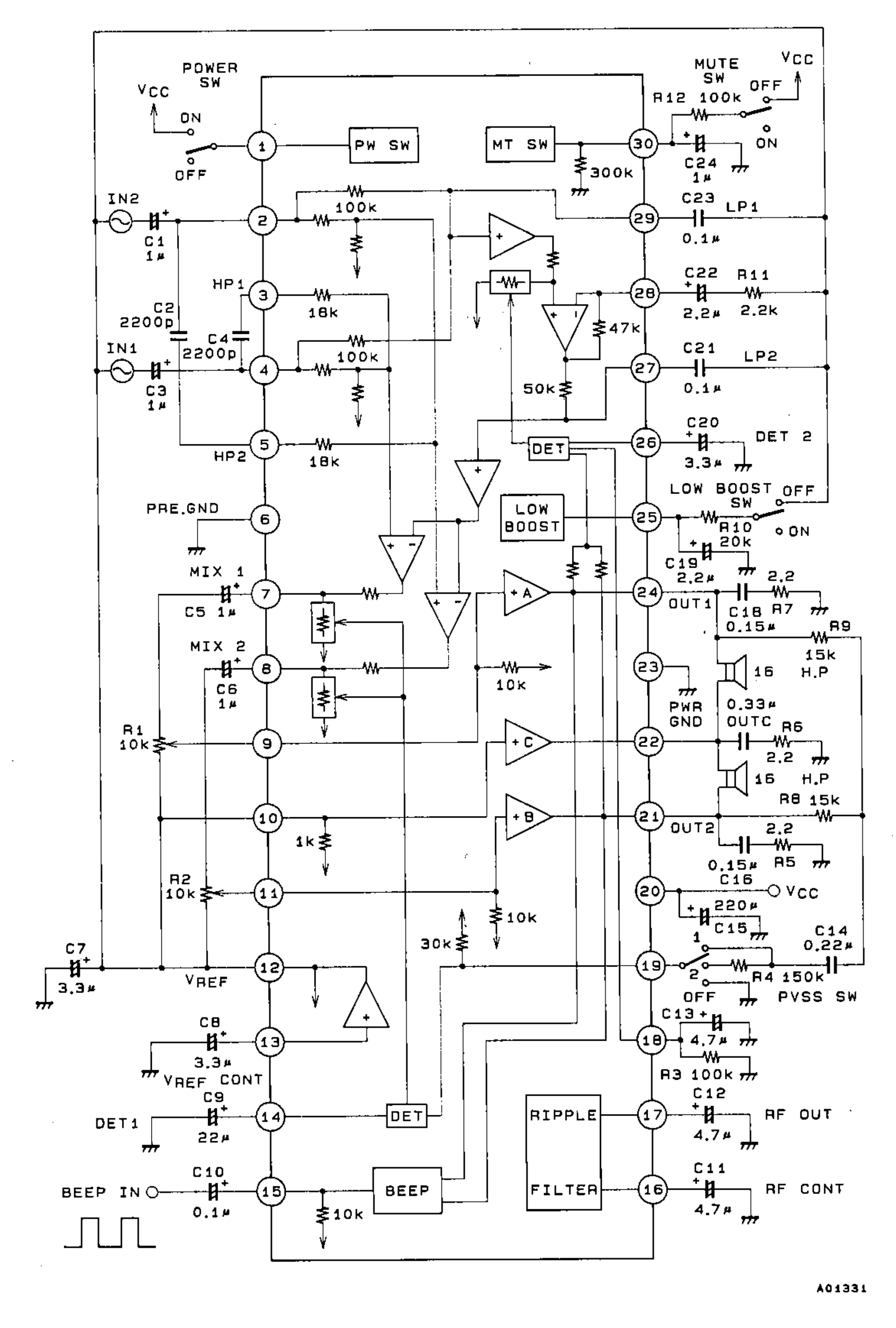
Unit (resistance: Ω)

Test Circuit



Unit (resistance: Ω, capacitance: F)

Application Circuit



Unit (resistance: Ω, capacitance: F)

Pin Functions and Equivalent Circuits (V_{CC} = 3.0 V)

Unit (resistance: Ω)

Pin No.	Symbol	V_{DC} (V)	Equivalent circuit	Pin function
1	PWR SW	0 to 0.7	A01332	• Applying V_{CC} to pin 1 turns the IC power on.
2 4	IN 2 IN 1	1.1 1.1	A01333	• Low boost input pin
3 5	H.P 1 H.P 2	1.1 1.1	A01334	• High-pass input pin
6	PRE GND			
7 8	MIX OUT 1 MIX OUT 2	1.1 1.1	A01335	• Low boost and buffer output pin
9 11	PWR IN 1 PWR IN 2	1.1 1.1	A01336	• Power input pin • The input resistance is 10 kΩ.
10	PWR IN C	1.1	A01337	• Power amp common input pin • Connect to Vref in normal operation

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Unit (resistance: Ω, capacitance: F)

Pin No.	Symbol	V_{DC} (V)	Equivalent circuit	Pin function
12	V_{REF} OUT	1.1	12, 300, 5p, A01338	• Fixed bias of 1.1 V
13	V_{REF} CONT	1.1	13, 300, 1k, 1k, A01339	• The V_{REF} CONT pin, 1.1 V
14	DET 1	0 to 1.3	To AVLS drive, VCC, 14, 300, 1k, 20k, A01340	• AVLS operates at 0.65 V or higher.
15	Beep IN	1.1	15, 300, 10k, A01341	• Beep input pin • Only operates when the muting function is on.
16	R.F CONT	2.2	16, 3.9k, 43k, 300, 36k, To R.F, A01342	• The R.F. CONT pin
17	R.F OUT	2.65	17, 3k, 300, 300, A01343	• Set to a bias of about 0.88 times V_{CC}.

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Unit (resistance: Ω, capacitance: F)

Pin No.	Symbol	V_{DC} (V)	Equivalent circuit	Pin function
18	PVSS S.C	0 to 0.7		• Smoothing pin used when PVSS is turned on and off.
19	PVSS SW	0 to 1.1		• PVSS is turned on by the power output signal, and turned off when grounded.
20	V_{CC}			
21 22 24	PWR OUT 2 PWR OUT C PWR OUT 1	1.1 1.1 1.1		• The power output pins • The LA4805V drives headphones with pin 22 used as a common center. (No electrolytic capacitors are used in the output.)
23	PWR GND			
25	LOW BOOST SW	0 to 1.0		• The low boost function is turned on when this pin is floating and turned off when it is connected to Vref.
26	DET 2	0.5 to 1.3		• ALC operates at 0.65 V or higher.
27	L.P 2	1.1		• Low boost secondary low pass pin

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Unit (resistance: Ω)

Pin No.	Symbol	V_{DC} (V)	Equivalent circuit	Pin function
28	LOW BOOST NF	1.1	28 300 47k A01350	• Low boost NF pin
29	L.P 1	1.1	29 300 100k To IN1 A01351	• Low boost primary low pass pin
30	MUTE SW	0 to 2.2	30 300 1k 1k 300k A01352	• The muting function is on when this pin is floating and off when connected to V_{CC} through a 100 kΩ resistor.

External Component Functions: Recommended values are indicated in parentheses.

• C1, C3 (1 to 4.7 μF)
Input coupling capacitors

• C2, C4 (2200 pF)
Input high pass capacitors. The high region gain when low boost is on is determined by the IC internal 18 kΩ resistance and these external 2200 pF capacitors.

• C5, C6 (0.1 to 1 μF)
Mixer amplifier to power amplifier coupling capacitors

• C7, C8 (3.3 to 10 μF)
Reference bias (Vref) decoupling capacitors

• C9 (10 to 22 μF)
Determines the PVSS recovery time.

• C10 (0.1 to 1 μF)
Beep input coupling capacitor. Be sure that this capacitor does not attenuate the beep signal.

• C11, C12 (4.7 to 10 μF)
Ripple filter capacitors. Care is required selecting their value, since although increasing the capacitance increases the ripple exclusion ratio, it also increases the rise time when the power is turned on.

• C13 (3.3 to 4.7 μF)
Smoothing capacitor for PVSS on/off switching noise

• C14 (0.22 to 0.47 μF)
Coupling capacitor that accepts the power output signal and inputs that signal to the PVSS function.

• C15 (220 μF)
Power supply line decoupling capacitor

• C16, C17, C18 (0.22 to 0.47 μF)
Oscillation suppression capacitors. We recommend using film capacitors.

• C19 (2.2 to 4.7 μF)
Smoothing capacitor for low boost on/off switching noise

• C20 (3.3 to 4.7 μF)
Determines the low boost attack time. Increasing the capacitance increases the attack time.

• C21, C23 (0.1 μF)
Low pass capacitors used with the low boost function

• C22 (2.2 to 4.7 μF)
Low boost amplifier NF capacitor. Values in excess of the recommended range will slow the low boost amplifier's rise time and may cause noise spikes.

• C24 (0.1 to 1.0 μF)
Determines the muting time. See the "IC Usage Notes" section for a discussion of the muting time when the capacitor C24 value is varied.

• R1, R2 (10 kΩ)
Mixer amplifier load resistance and power input adjustment potentiometer.

• R3 (100 k to 1 MΩ)
Smoothing resistor for PVSS on/off switching noise

• R4 (50 k to 200 kΩ)
PVSS level adjustment resistor

• R5, R6, R7 (1 to 4.3 Ω)
Power amplifier oscillation suppression capacitors. We recommend using film capacitors.

• R8, R9 (15 kΩ)
Power output signal bias resistor for PVSS operation

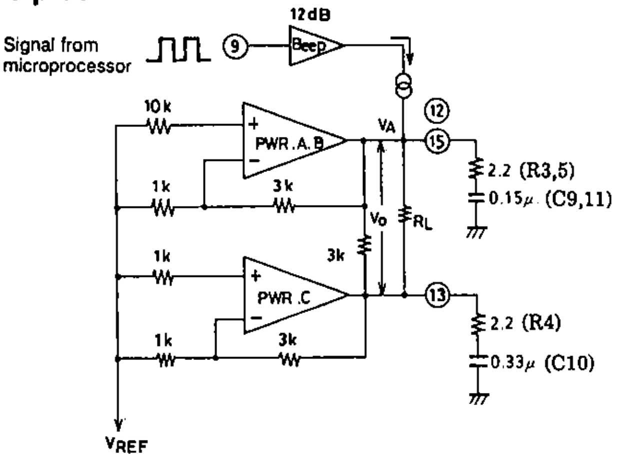
• R10 (20 kΩ)
Determines the pin 25 bias when low boost is off.

• R11 (1.5 k to 2.2 kΩ)
Determines the low boost amplifier's voltage gain.

• R12 (100 kΩ)
Determines the pin 30 bias when muting is off (and PWR is on).
We recommend using a 100 kΩ resistor for R12, since the muting switch pin (pin 30) threshold area is determined by this (100 kΩ) resistance and the IC's internal 300 kΩ resistance.

Usage Notes and Operating Principles

1. Beep function operating principles



Unit (resistance: Ω, capacitance: F)

- The figure above shows the beep function block, which is designed to operate when muting is on, i.e., when pin 16 is open.
  The output voltage generated at R_L at that time is given by the following equation.

$$V_O = \frac{R_L}{R_L + 3\,k + 1\,k} \times V_A$$

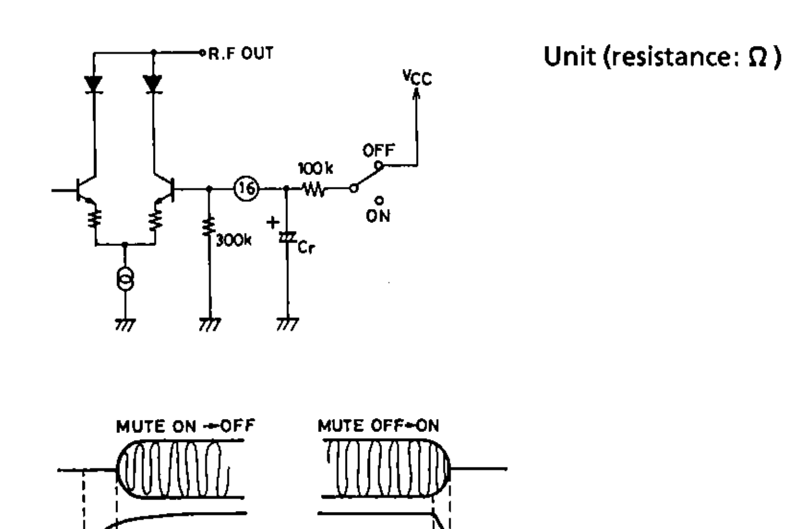
  For example, when R_L is 16 Ω and V_A is 0.5 V: (V_A is adjusted by the pin 9 input level.)

$$V_O = \frac{16\,\Omega}{16\,\Omega + 3\,k + 1\,k} \times 0.5\ V \approx 2\ mV$$

- While the beep output V_O is determined by the formula above, it is influenced by the capacitor and resistor used to form the PWR output oscillation suppression function. Therefore, when using the beep function, it is necessary to make the impedance due to the pin 13 capacitor C10 smaller than the impedance of capacitors C9 and C10 on pins 12 and 15, since pin 13 is a common output. Which is to say, the capacitor C10 must be larger than the capacitors C9 and C10.

2. Muting time

Unit (resistance: Ω)

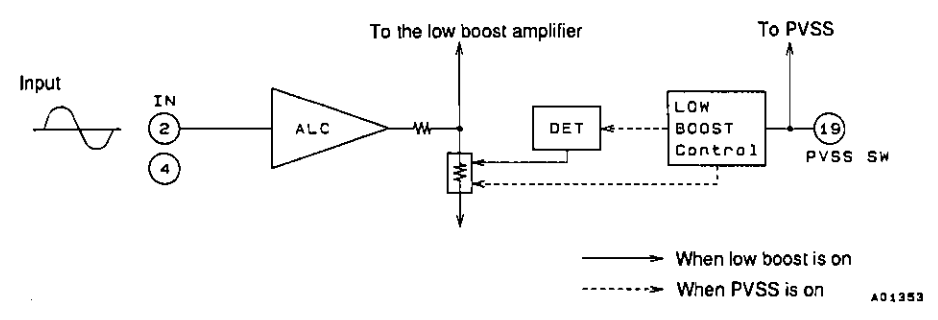


- The figure above shows the waveform when the muting function is turned on and off. The ts on and off times here can be changed by the capacitor Cr on pin 16. While the recommended value for Cr is 1 μF, note that reducing this value can lead to increased impulse ("pop") noise.

- The table below lists the ts on and off times for different values of Cr.

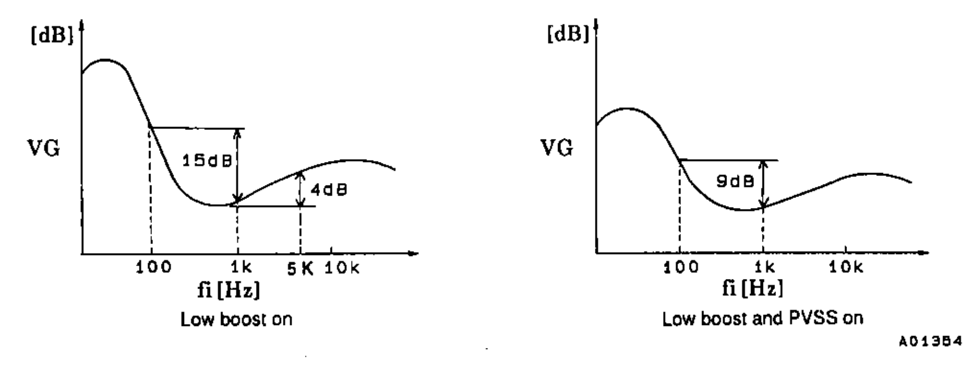
Cr	ts OFF	ts ON
0.1 μF	15 ms	3.2 ms
1.0 μF	150 ms	30 ms
2.2 μF	300 ms	56 ms

3. Boost level when the low boost function and PVSS are on

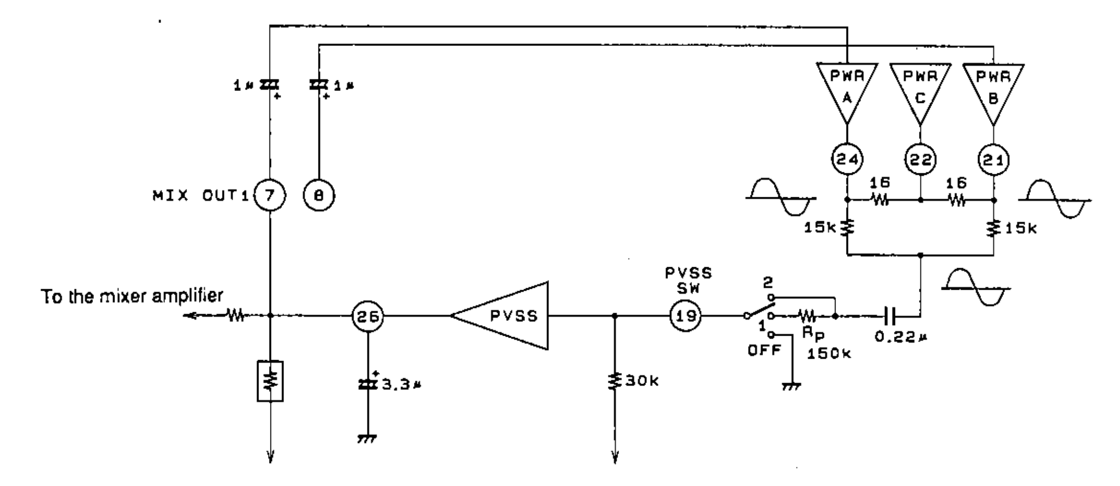


- Normally, the 100 Hz boost level with respect to 1 kHz is 15 dB when low boost is on. However, the LA4805V is designed so that the 100 Hz boost level with respect to 1 kHz is 9 dB when both PVSS and low boost are on. PVSS is turned on when the power output is input to pin 19, and the low boost level is determined by adjusting the DET as shown by the dotted lines in the figure. (See the separately provided detailed data describing the state where both low boost and PVSS are on.)

- The graphs below give a simplified view of the fi-VG characteristics.

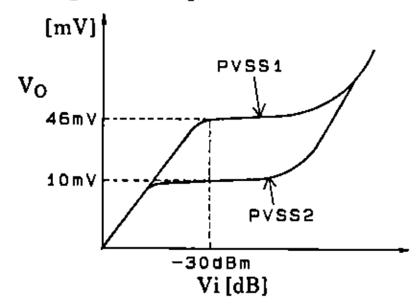


4. PVSS

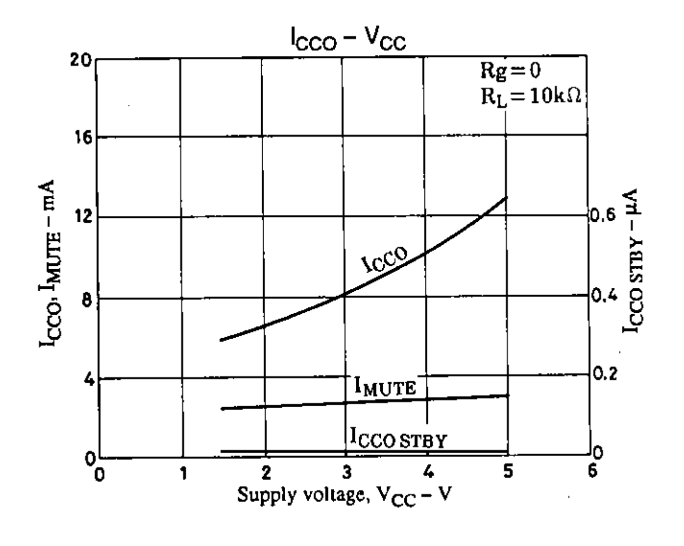


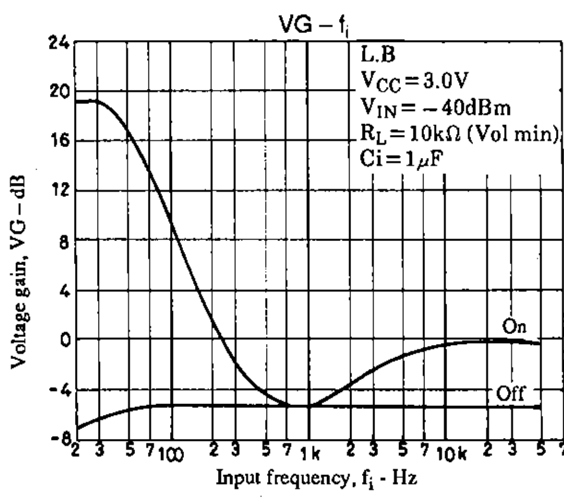
Unit (resistance: Ω, capacitance: F)

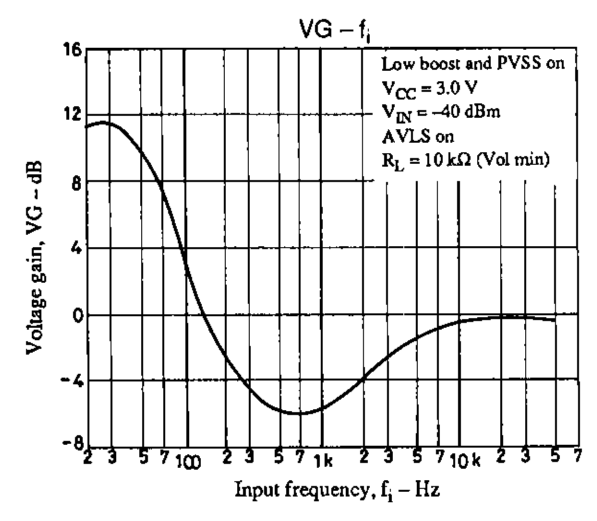
- As shown in the figure above, PVSS is designed so that PVSS is operated and turned on by inputting to pin 19 the mixed power outputs through 15 kΩ resistors. When this input is grounded, PVSS is turned off.
- PVSS switching can be changed by an IC internal 30 kΩ resistor and an external (150 kΩ) resistor. When this function is used, V_O is set to 45 mV by passing the mixed signal through a 150 kΩ resistor at PVSS1, and is set to 10 mV by passing the mixed signal through only the 0.22 μF capacitor at PVSS2. (Detailed data is provided separately.)
- The graph below gives a simplified view of the Vi-V_O characteristics and the output V_O when R_P is varied.

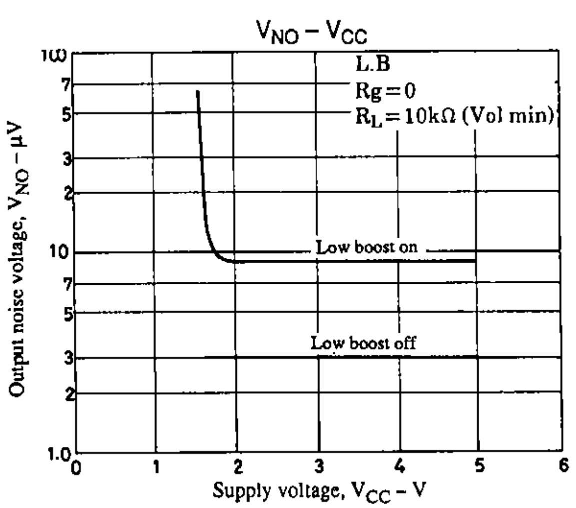


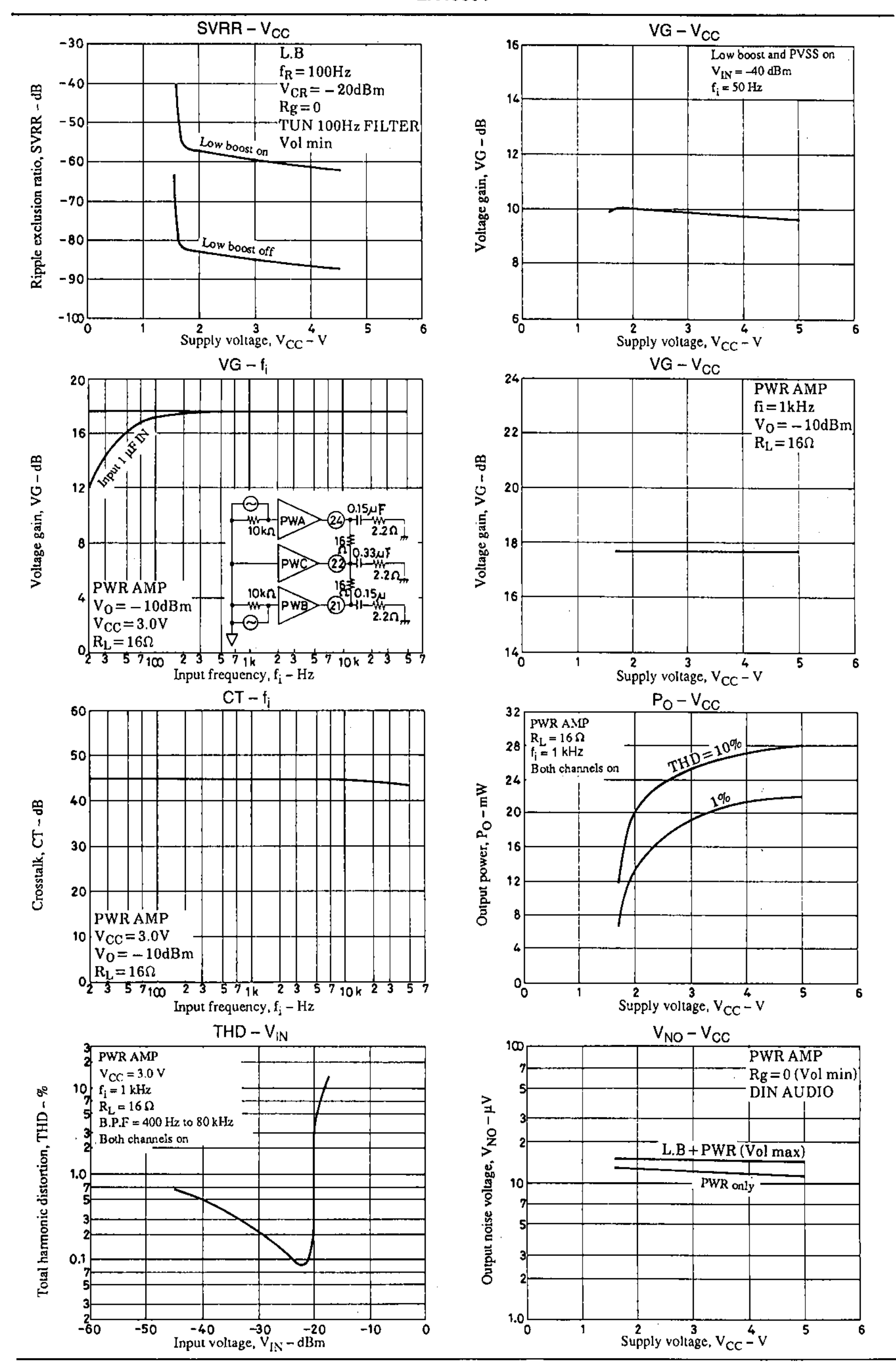
R_P	V_O
50 kΩ	25 mV
100 kΩ	35 mV
150 kΩ	46 mV
200 kΩ	56 mV

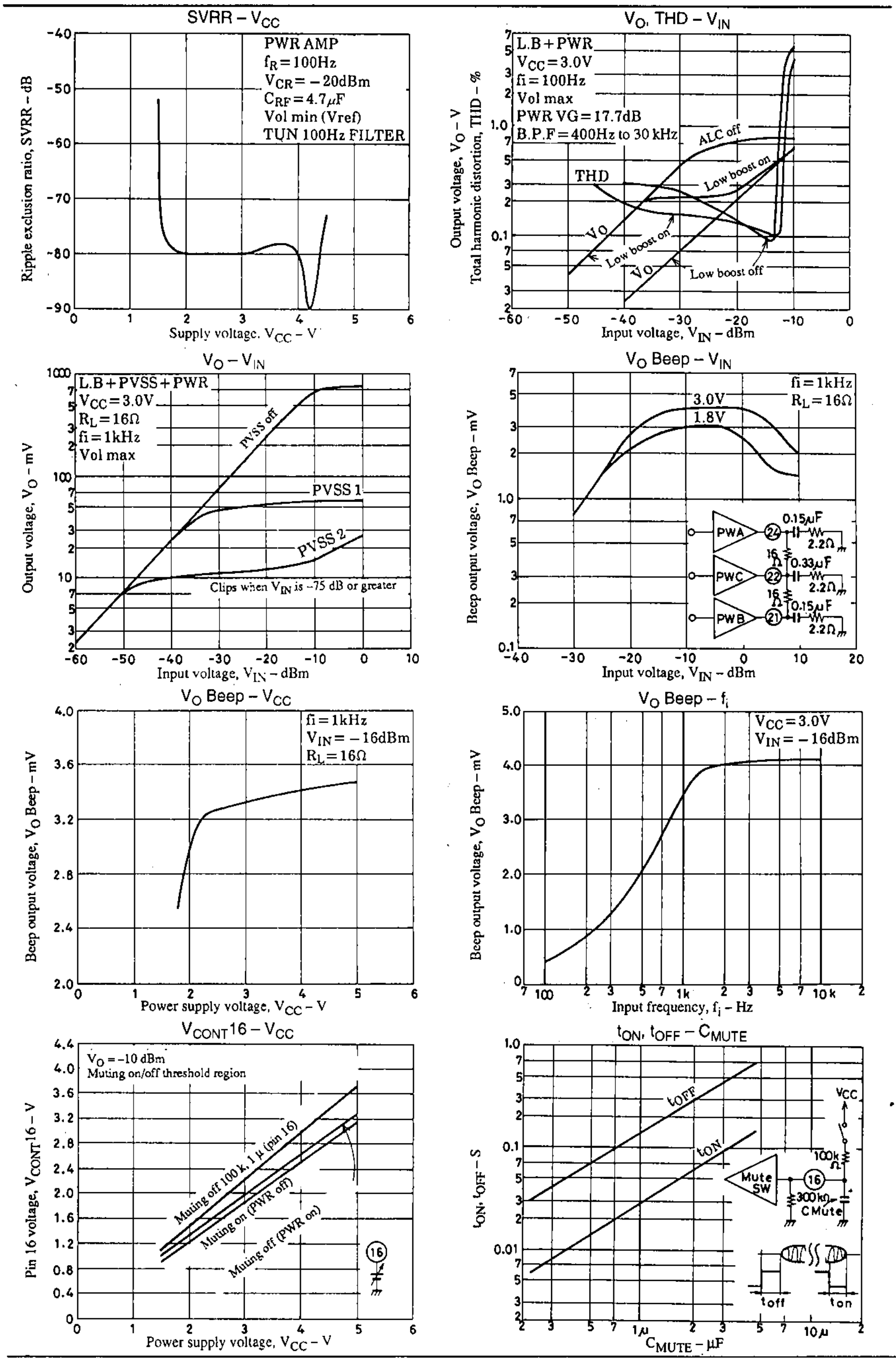


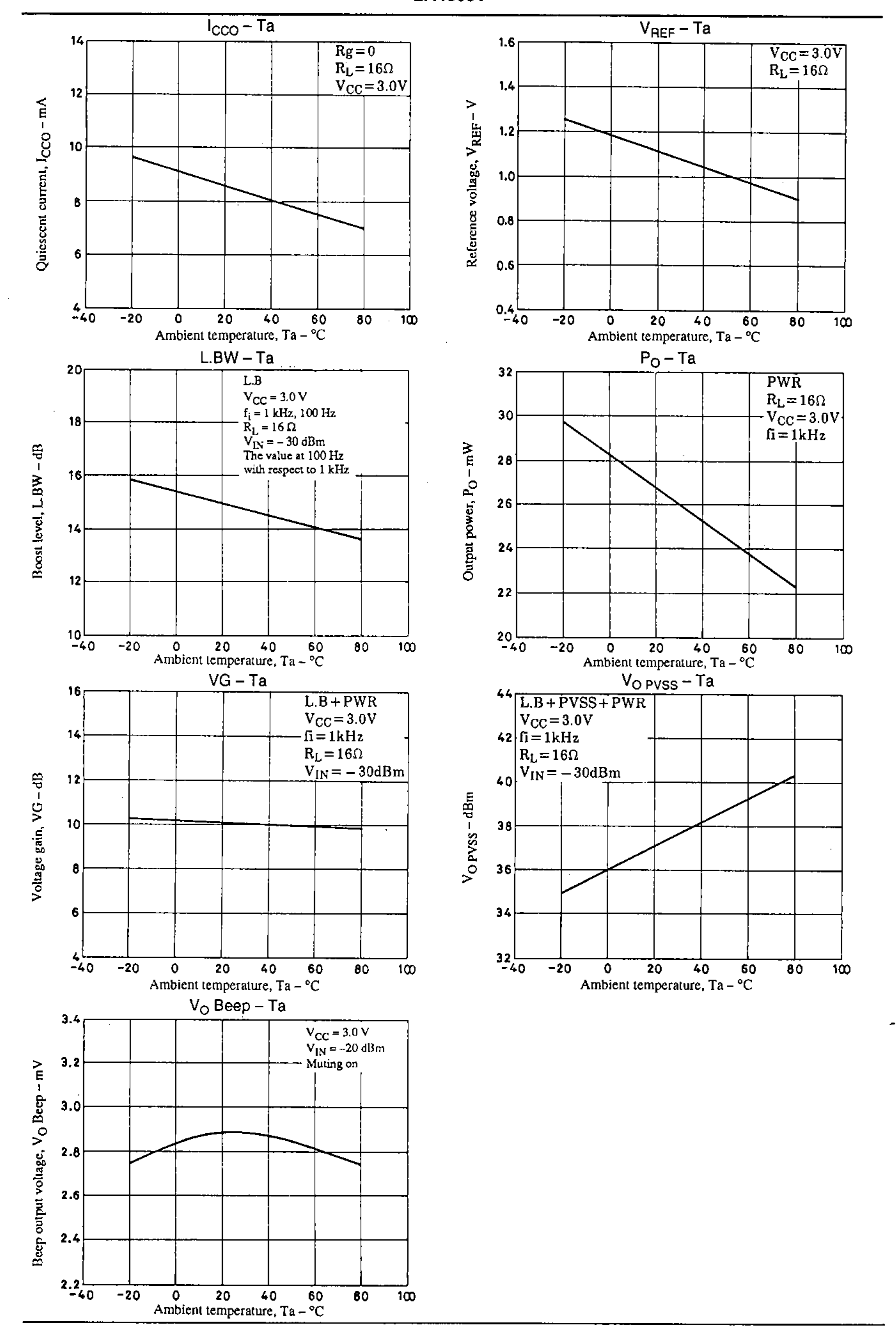







SVRR – VCC
L.B
fR = 100Hz
VCR = –20dBm
Rg = 0
TUN 100Hz FILTER
Vol min
Low boost on
Low boost off
Ripple exclusion ratio, SVRR – dB
Supply voltage, VCC – V
VG – VCC
Low boost and PVSS on
VIN = –40 dBm
fi = 50 Hz
Voltage gain, VG – dB
Supply voltage, VCC – V
VG – fi
Input 1 μF IN
PWR AMP
VO = –10dBm
VCC = 3.0V
RL = 16Ω
PWA
PWC
PWB
10kΩ
0.15μF
0.33μF
0.15μ
2.2Ω
16
Voltage gain, VG – dB
Input frequency, fi – Hz
VG – VCC
PWR AMP
fi = 1kHz
VO = –10dBm
RL = 16Ω
Voltage gain, VG – dB
Supply voltage, VCC – V
CT – fi
PWR AMP
VCC = 3.0V
VO = –10dBm
RL = 16Ω
Crosstalk, CT – dB
Input frequency, fi – Hz
PO – VCC
PWR AMP
RL = 16 Ω
fi = 1 kHz
Both channels on
THD = 10%
1%
Output power, PO – mW
Supply voltage, VCC – V
THD – VIN
PWR AMP
VCC = 3.0 V
fi = 1 kHz
RL = 16 Ω
B.P.F = 400 Hz to 80 kHz
Both channels on
Total harmonic distortion, THD – %
Input voltage, VIN – dBm
VNO – VCC
PWR AMP
Rg = 0 (Vol min)
DIN AUDIO
L.B + PWR (Vol max)
PWR only
Output noise voltage, VNO – μV
Supply voltage, VCC – V


SVRR – VCC
PWR AMP
fR = 100Hz
VCR = –20dBm
CRF = 4.7μF
Vol min (Vref)
TUN 100Hz FILTER
Ripple exclusion ratio, SVRR – dB
Supply voltage, VCC – V
VO, THD – VIN
L.B + PWR
VCC = 3.0V
fi = 100Hz
Vol max
PWR VG = 17.7dB
B.P.F = 400Hz to 30 kHz
ALC off
Low boost on
THD
Low boost off
Output voltage, VO – V
Total harmonic distortion, THD – %
Input voltage, VIN – dBm
VO – VIN
L.B + PVSS + PWR
VCC = 3.0V
RL = 16Ω
fi = 1kHz
Vol max
PVSS off
PVSS 1
PVSS 2
Clips when VIN is –75 dB or greater
Output voltage, VO – mV
Input voltage, VIN – dBm
VO Beep – VIN
fi = 1kHz
RL = 16Ω
3.0V
1.8V
PWA
PWC
PWB
0.15μF
0.33μF
2.2Ω
Beep output voltage, VO Beep – mV
Input voltage, VIN – dBm
VO Beep – VCC
fi = 1kHz
VIN = –16dBm
RL = 16Ω
Beep output voltage, VO Beep – mV
Power supply voltage, VCC – V
VO Beep – fi
VCC = 3.0V
VIN = –16dBm
Beep output voltage, VO Beep – mV
Input frequency, fi – Hz
VCONT16 – VCC
VO = –10 dBm
Muting on/off threshold region
Muting off 100 k, 1 μ (pin 16)
Muting on (PWR off)
Muting off (PWR on)
Pin 16 voltage, VCONT16 – V
Power supply voltage, VCC – V
tON, tOFF – CMUTE
tOFF
tON
VCC
100k
Mute SW
300kΩ
CMute
toff
ton
tON, tOFF – S
CMUTE – μF



I_{CCO} – Ta
Rg=0
R_L=16Ω
V_{CC}=3.0V
Quiescent current, I_{CCO} – mA
Ambient temperature, Ta – °C
V_{REF} – Ta
V_{CC}=3.0V
R_L=16Ω
Reference voltage, V_{REF} – V
Ambient temperature, Ta – °C
L.BW – Ta
L.B
V_{CC} = 3.0 V
f_i = 1 kHz, 100 Hz
R_L = 16 Ω
V_{IN} = – 30 dBm
The value at 100 Hz
with respect to 1 kHz
Boost level, L.BW – dB
Ambient temperature, Ta – °C
P_O – Ta
PWR
R_L=16Ω
V_{CC}=3.0V
fi=1kHz
Output power, P_O – mW
Ambient temperature, Ta – °C
VG – Ta
L.B+PWR
V_{CC}=3.0V
fi=1kHz
R_L=16Ω
V_{IN}= – 30dBm
Voltage gain, VG – dB
Ambient temperature, Ta – °C
$V_{O\ PVSS}$ – Ta
L.B+PVSS+PWR
V_{CC}=3.0V
fi=1kHz
R_L=16Ω
V_{IN}= – 30dBm
$V_{O\ PVSS}$ – dBm
Ambient temperature, Ta – °C
V_O Beep – Ta
V_{CC} = 3.0 V
V_{IN} = –20 dBm
Muting on
Beep output voltage, V_O Beep – mV
Ambient temperature, Ta – °C